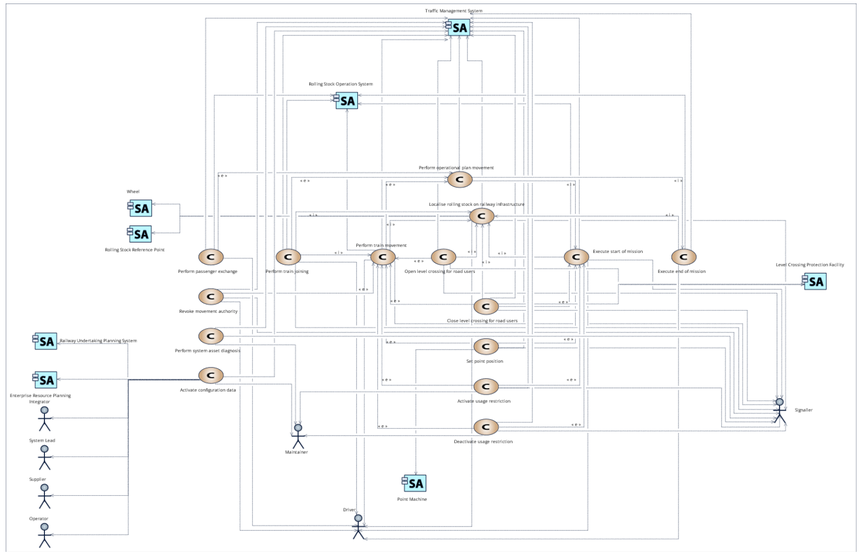
Task 2: Architecture

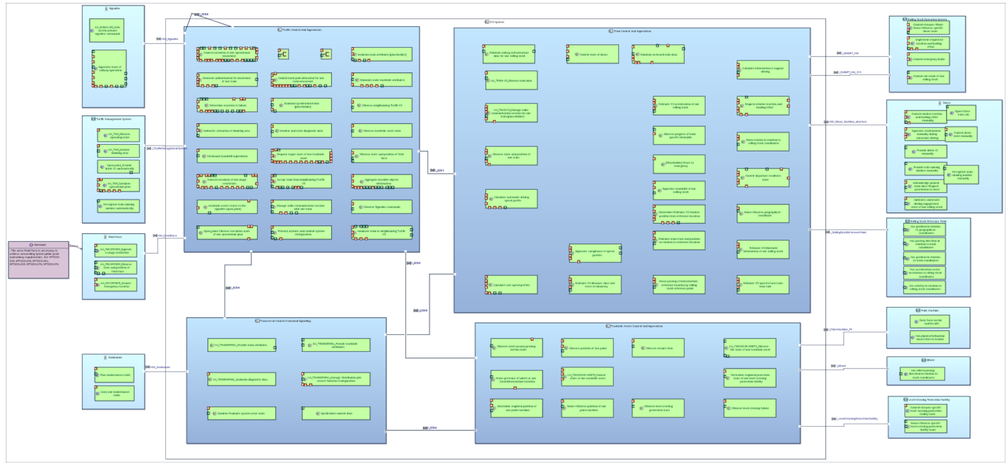
T2 ARC domain is responsible for the “coordination areas”. Each coordination issue is not a design task per se, but fulfils a cross-domain, cross-task and SP-IP oriented roles, supported by the SP Core-group.

The generic target of the coordination is to provide the information for **external communication** and **Task 2 internal management** of a cross-domain, cross-task or SP-IP issues. The second target is a faster decision process, by collating the necessary information to allow key architectural questions to be answered.

CCS System Capability (Version 1)



Target CCS Logical Architecture (Version 1)



The Functional Architecture Team (ARC-F) will focus on developing the following new functions and technical enablers for the **“Harmonized European Rail Operation” migration plateau**:

- ETCS L2 Functionality based on System Version 2.3 or higher
- CCS Architecture based on: Harmonized Trackside Protection System ("TPS", combining a cleaned-up interlocking and RBC functionality specialized on ETCS L2) and Plan Execution System (“PE”; EAL)
- Safe traffic control for mixed traffic with trains with or without train integrity/train length information;
- Supervised maneuvers and harmonized ETCS shunting signals as implem. option
- All other interfaces of the System Pillar Target Architecture, which are perhaps agreed and published at this time, can be used for optional implementations

ARC-F will also focus on developing the following new functions and technical enablers for a “**Digital European Railway**” and an **“Automated European Railway”**:

- Automatic Train Operation Grade of Automation to level 3 and 4
- Harmonized Remote Train Operation functionality (optional)

Task 2: ARC

Lead STIP Deliverables

- **STIP_5: High level logical architecture on system level 3: Names of the subsystems and interfaces -** 2024
- **STIP_135: ETCS CR enhancements – completion dates are defined in the Standardisation and TSI Input Plan (STIP)**

Deliverables Request for Service (SC2.4) – Year 3 [Oct-24 – Oct-25]

D01 **ATP/ETCS overview -** Sept 2025

D02 **TSI CR Overview** – Continuous

D03 **High level logical architecture on System Level 3** – Continuous

D04 **System Pillar Document and Release Plan ("DRP")** – Continuous

D05 **Support to the EGNOS Project** – Dec 2025

Latest Achievements, Challenges and Design Decisions

Latest Achievements: The following achievements have been accomplished by ARC domain:

- **Achievement #1:** ETCS Change Request process integrated into CCM process and following the STIP change requests are being processed as planned.
- **Achievement #2:** On-boarding of the Domains and Tasks on SP Release production. Setup of the list of the SP documents to be delivered as part of the SP Release in 10/2025. This SP Release will be referenced by the call of tender of Innovation Pillar Wave 2. The list of SP documents will be communicated by April 20th to the Core Group.
- **Achievement #3:** CR preassessment bundles "CCS stepwise system evolution", "ASTP", "OB Modulrity", "Cyber Security", "Train Interface" and "Authorisation and Upgradeability" sent to ERA.
- **Achievement #4:** As basis for discussion with R2DATO a planning and assignment of responsibilities has been drafted, proposed and was presented in the last plenary SP/R2DATO, link: CR Bundles Planning IP SP v05.xlsx

- **Domain Current challenges:** The domain is facing the following challenges:
  - **Challenge #1:** Update of the CR preassessment bundles based on the ERA comments until end of May. Reorganisation with new roles and members for ARC2.4.
  - **Challenge #2:** At the moment, Overall Consist Length is not considered in IP
  - **Challenge #3:** Update of the Architecture Roadmap based on the updated STIP.
- **Design Decisions:** The domain has made the following design decisions that impact the Overall Model:
  - functional allocation on higher level (aka System Level 3) is finalized on CCS level.

Expected outcomes for sector review in the next 3 months

- **The next review will be in Q2/2025: Complete System Level 3 architecture**